

REMARKS/ARGUMENTS

Entry of this amendment and reconsideration of the present application, as amended, are respectfully requested.

Claims 1-28 are pending in this application and all were rejected. Claims 1, 21 and 22 are amended. Unless an argument is made below relating to the patentability of each of these claims over cited prior art, the changes to the claims do not relate to patentability.

The courtesies extended by the Examiner in a telephonic interview on July 6, 2006 are gratefully appreciated.

Specification

The Examiner objected to the amendment filed November 14, 2005 because it introduces new matter, specifically, the amendment to the specification.

The portion added by the amendment filed November 14, 2005, and indicated by the Examiner to constitute new matter, has been removed to expedite prosecution and without acknowledging that it is indeed new matter.

In view of the changes to the specification, it is respectfully submitted that the Examiner's objection has been overcome and should be removed.

Drawings

The drawings were objected to under 37 C.F.R. §1.83(a) on the grounds that the features of "signals between a form processable by the at least one video device but unprocessable by said video generator and analyzer and a form processable by said video generator and analyzer but unprocessable by the at least one video device" and "overlaying of grids" are not shown.

Claims 1 and 21 have been amended to amend the feature of the signal conversion by the signal conditioner/switching device. It is respectfully submitted that the current features in claims 1 and 21 are present in the drawings, and specifically Fig. 2, in view of the repeated use of terms which conveys modification of signals to one of ordinary skill in the art. These terms including "scaling", "AC to DC", "level shift to PECL", "impedance matching" and others as set forth in Fig. 2.

Claim 22 is amended to remove mention of the "overlaying of grids" and to recite the function of the analysis tools as method limitations.

In view of the foregoing, it is respectfully submitted that the Examiner's objection to the drawings has been overcome and should be removed.

Claim Rejections-35 U.S.C. § 112

Claims 1-27 were rejected under 35 U.S.C. §112, first paragraph, and under 35 U.S.C. §112, second paragraph, on the grounds that it was not clear what was meant by the signal conversion feature in claims 1 and 21.

Initially, it is pointed out that claims 1 and 21 are amended to clarify the signal conversion feature and now recite that the signals from the video source are modified and then provided to the video generator and analyzer, i.e., a signal modification feature.

The specification as originally filed and the content of Fig. 2 adequately disclose modification of an input signal from the video source with the modified signal being provided to the video generator and analyzer. The tables below show different types of input signals which are modified by one of the emulators described in the specification with the modified signals then being directed to the portable video generator and analyzer and the location for support in the originally filed specification.

Digital Multimeter Emulator (52)

UUT signal unprocessable by PVGA due to	Modification by SC/SD emulator	Support in specification as originally filed	Resulted signal processable by PVGA
Voltage out of range	Scaling – amplification or attenuation	Page 8, lines 12- 14 and Figure 2	Signal within +/- 10 VDC range
Signal is AC (sinewave)	AC to DC converter	Figure 2	Signal within +/- 10 VDC range
Signal is AC (non-sinewave)	AC to RMS converter	Page 8, lines 15-16 and Figure 2	Signal within +/- 10 VDC range
Resistance	Current source to produce a proportional voltage	Page 8, lines 16-17 and Figure 2	Signal within +/- 10 VDC range

DME 52 in Fig. 2 clearly shows “scaling”, “AC to DC”, “RMS” and “current source” which would be understood by one skilled in the art as the functions being performed by the DME, especially when considered in light of the specification at page 8, lines 6-17.

Counter Timer Emulator (54)

UUT signal unprocessable by PVGA due to	Modification by SC/SD emulator	Support in specification as originally filed	Resulted signal processable by PVGA
Logic level not PECL (Positive Emitter Coupled Logic)	Programmable logic level converter with differential PECL output	Page 9, lines 7–10 and Figure 2	Differential PECL
UUT signal differential (non-PECL)	Differential receiver with differential PECL outputs	Page 9, lines 10-11 and Figure 2	Differential PECL
Frequency out of range - too high	Prescaling	Page 9, line 10-11 and Figure 2	Frequency in range
Time interval too long	Divide-by-N to extend range of the time interval	Page 9, lines 11-12 and Figure 2	Time interval within range

CTE 54 in Fig. 2 clearly shows “level shift to PECL”, “prescaling”, “divide by N” and “diff. RCVR” which would be understood by one skilled in the art as the functions being performed by the CTE, especially when considered in light of the specification at page 9, lines 7-12. Also note that the specification expressly recites that the CTE will “translate the input level to differential PECL”, with such translation constituting a modification.

Digitizer/Oscilloscope Emulator (56)

UUT signal unprocessable by PVGA due to	Conversion by SC/SD emulator	Support in specification as originally filed	Resulted signal processable by PVGA
Analog trigger signal	Variable threshold/polarity comparator	Page 9, lines 16-17 and Figure 2	TTL level digital trigger
No internal PVGA gate timer	Programmable gate timer	Page 9, line 20 and Figure 2	TTL level digital gate of correct duration
No internal PVGA gate delay	User-specified delay	Page 9, lines 22–23	TTL level digital gate with correct delay
UUT Signal too large or small	Scaling	Figure 2	Signal in +/- 10 V range

DOE 56 in Fig. 2 clearly shows “scaling”, “trigger level” and “trigger slope” which would be understood by one skilled in the art as the functions being performed by the DOE, especially when considered in light of the specification at page 9, lines 11-23.

Pulse Generator Buffer (58)

PVGA signal unprocessable by UUT due to	Modification by SC/SD emulator	Support in specification as originally filed	Resulting signal processable by UUT
UUT load requires current more than PVGA can provide	Buffer	Page 10, lines 1-2 and Figure 2	Sufficient current is provided
UUT load requires voltage more than PVGA can provide	Scaling	Page 9, line 30-page 10, line 1 and Figure 2	Voltage is adjusted to meet UUT requirements.
UUT load impedance different than PVGA output impedance	Impedance matching	Page 10, lines 1-2 and Figure 2	Signal has correct impedance as required by the UUT

PGB 58 in Fig. 2 clearly shows “scaling”, “impedance matching” and “buffer” which would be understood by one skilled in the art as the functions being performed by the PGB, especially when considered in light of the specification at page 9, lines 24-30. Also note that the specification at page 9, lines 28-29, expressly recites that the PGB will “accept the TTL level inputs and level shift then to user-specified voltages”, with such level shifting constituting a modification.

In sum, the pending claims recite modification of signals between the video source and the video generator and analyzer and the specification as originally filed provides numerous examples of how this modification is performed.

In view of the foregoing, it is respectfully submitted that the Examiner’s rejections of claims 1-27 under 35 U.S.C. §112, first and second paragraphs, have been overcome and should be removed.

Claim Rejections-35 U.S.C. §102

Claim 28 was rejected under 35 U.S.C. §102(b) as being anticipated by Howell et al. (US 6,396,536 B1), hereinafter Howell. The Examiner states that Howell includes a signal conditioner/switching device including elements 16, 18, 20 which he considered to be a digitizer/oscillator emulator, a digital multi-meter emulator and a counter/timer emulator.

The Examiner’s rejection is respectfully traversed.

An emulator may be considered an electrical device which imitates the function of another system, as by modifications to hardware or software that allow the imitating system to accept the same data, execute the same programs, and achieve the same results as the imitated

system. Thus, a digitizer/oscillator emulator is a device which imitates the function of a digitizer/oscillator, a digital multi-meter emulator is a device which imitates the function of a digital multi-meter and a counter/timer emulator is a device which imitates the function of a counter/timer.

Elements 16, 18, 20 in Howell are a primary composite video generator 16, a secondary video source 18 and a stroke generator 20. The primary composite video 16 is arranged to produce video in a wide array of standard and non-standard formats (see col. 5, lines 15-56). The secondary video source 18 is arranged to generate composite video in any format (see col. 13, lines 24-17). The stroke generator 20 is arranged to generate stroke, or X-Y-Z, video (see col. 10, line 65 to col. 12, line 2).

There does not appear to be any description of primary composite video 16 imitating or emulating a digitizer/oscilloscope, secondary video source 18 imitating or emulating a digital multi-meter or stroke generator 20 imitating or emulating a counter/timer.

As such, Howell does not disclose, teach or suggest providing one or more emulators in a signal conditioner/switching device which is included in a portable automatic video test analyzer.

In view of the foregoing, it is respectfully submitted that the Examiner's rejection of claim 28 has been overcome and should be removed.

Petition for Extension

Applicant hereby petitions for a two-month extension of time to extend the time for response to the Office Action for two months from June 17, 2006 to August 17, 2006.

An early and favorable action on the merits upon entry and consideration of this amendment is earnestly solicited.

FOR THE APPLICANT
Respectfully submitted,

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